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=> d his

        (FILE 'USPAT' ENTERED AT 13:59:58 ON 28 AUG 1997)
L1          509 S ((MULTI-PRECISION OR PRECISION)(3A)ARITHMETIC)
L2          404 S L1 AND (PROCESSOR# OR CPU#)
L3          391 S L2 AND (MEMORY OR RAM OR STORAGE OR REGISTER#)
L4          342 S L3 AND (BOOLEAN OR INTEGER OR FLOATING-POINT OR FLOATING
PO
L5          283 S L4 AND ((TRANSFER? OR TRANSMIT? OR SEND? OR RECEIV?)(5A)
DAT
L6          154 S L5 AND (DATA(3A)(SIZE# OR LENGTH# OR WIDTH#))
L7           69 S L6 AND ((DATA OR PEAK)(2A)(RATE# OR THROUGHPUT OR CAPACI
TY)
L8           66 S L7 AND (PATH# OR CHANNEL#)
L9           34 S L6 AND (ARITHMETIC OR MATHEMAT?)/TI,AB
L10          14 S L9 NOT L7
L11          11 S L6 AND (MEDIA(3A)(DATA OR INFORMATION OR PROCESSOR# OR C
PU#
L12          80 S (L8 OR L10)
L13           7 S L11 NOT L12
L14          87 S (L12 OR L13)
L15          12 S L1 AND (MEDIA(3A)(DATA OR INFORMATION OR PROCESSOR# OR C
PU#
L16           1 S L15 NOT L14
L17          88 S (L14 OR L16)
L18        5048 S (ARITHMETIC OR MATHEMAT?)/TI,AB
L19         180 S L18 AND (MULTIPRECISION OR MULTI-PRECISION OR DOUBLE PRE
CIS
L20         114 S L19 AND (PROCESSOR# OR CPU# OR EXECUT? OR MEDIA OR MANIP
ULA
L21         104 S L20 NOT L17
L22          51 S L21 AND ((DATA OR COMMUNICATION OR TRANSMISSION)(2W)(PAT
H#
L23          89 S L20 AND (INTEGER OR FLOATING POINT OR FLOATING-POINT)
L24          49 S L23 AND (RATE OR THROUGHPUT)
L25          77 S (L22 OR L24)
L26          70 S L25 NOT L17
L27         158 S (L17 OR L26)
L28         107 S L27 AND (PROCESSOR# OR CPU# OR MEDIA OR RATE OR THROUGHP
UT

=> d 1-107
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1. 5,659,495, Aug. 19, 1997, Numeric **processor** including a
multiply-add circuit for computing a succession of product sums using
redundant values without conversion to nonredundant format; Willard
Stuart Briggs, et al., 364/736.02, 746.2 :IMAGE AVAILABLE:

2. 5,644,524, Jul. 1, 1997, Iterative division apparatus, system and
method employing left most one's detection and left most one's detection
with exclusive or; Jerry R. Van Aken, et al., 364/766 :IMAGE AVAILABLE:

3. 5,644,522, Jul. 1, 1997, Method, apparatus and system for multiply
rounding using redundant coded multiply result; Philip Moyse, et al.,
364/745.02, 746.2 :IMAGE AVAILABLE:

4. 5,640,588, Jun. 17, 1997, **CPU** architecture performing dynamic
instruction scheduling at time of **execution** within single clock

cycle; Anantakotiraju Vasesna, et al., 395/800.23; 364/230.3, 231.8, 262.4, DIG.1; 395/390, ● :IMAGE AVAILABLE: ●

5. 5,625,836, Apr. 29, 1997, SIMD/MIMD processing memory element (PME); Thomas N. Barker, et al., 395/200.44, 377, 474 :IMAGE AVAILABLE:

6. 5,606,677, Feb. 25, 1997, Packed word pair multiply operation forming output including most significant bits of product and other bits of one input; Keith Balmer, et al., 395/384; 364/757, DIG.1, DIG.2 :IMAGE AVAILABLE:

7. 5,606,374, Feb. 25, 1997, Video receiver display of menu overlaying video; Randal L. Bertram, 348/565; 345/114, 158; 348/601, 734 :IMAGE AVAILABLE:

8. 5,604,544, Feb. 18, 1997, Video receiver display of cursor overlaying video; Randal Lee Bertram, 348/601; 345/158; 348/563, 734 :IMAGE AVAILABLE:

9. 5,602,597, Feb. 11, 1997, Video receiver display of video overlaying menu; Randal L. Bertram, 348/565; 345/114, 158; 348/601, 734 :IMAGE AVAILABLE:

10. 5,600,847, Feb. 4, 1997, Three input arithmetic logic unit with mask generator; Karl M. Guttag, et al., 395/800.36; 364/DIG.1; 395/501, 800.34 :IMAGE AVAILABLE:

11. 5,600,846, Feb. 4, 1997, Data processing system and method thereof; Michael G. Gallup, et al., 395/800.05, 800.03, 800.06 :IMAGE AVAILABLE:

12. 5,600,726, Feb. 4, 1997, Method for creating specific purpose rule-based n-bit virtual machines; Joseph M. Morgan, et al., 380/49, 4, 25 :IMAGE AVAILABLE:

13. 5,598,571, Jan. 28, 1997, Data processor for conditionally modifying extension bits in response to data processing instruction execution; Michael G. Gallup, et al., 395/800.09; 364/931.03, 931.51, 944.4, 944.6, 946.7, DIG.2; 395/800.03, 800.22 :IMAGE AVAILABLE:

14. 5,590,350, Dec. 31, 1996, Three input arithmetic logic unit with mask generator; Karl M. Guttag, et al., 395/800.36; 364/DIG.1, DIG.2; 395/501, 800.34 :IMAGE AVAILABLE:

15. 5,590,345, Dec. 31, 1996, Advanced parallel array processor(APAP); Thomas N. Barker, et al., 395/800.11; 364/DIG.1, DIG.2; 395/800.14, 800.15 :IMAGE AVAILABLE:

16. 5,588,152, Dec. 24, 1996, Advanced parallel processor including advanced support hardware; Michael C. Dapp, et al., 395/800.16 :IMAGE AVAILABLE:

17. 5,583,805, Dec. 10, 1996, Floating-point processor having post-writeback spill stage; Timothy A. Elliott, et al., 364/748.01 :IMAGE AVAILABLE:

18. 5,572,689, Nov. 5, 1996, Data processing system and method thereof; Michael G. Gallup, et al., 395/376; 364/DIG.2 :IMAGE AVAILABLE:

19. 5,561,617, Oct. 1, 1996, Pyramid processor integrated circuit; Gooitzen S. van der Wal, 364/724.05, 724.13 :IMAGE AVAILABLE:

20. 5,559,973, Sep. 24, 1996, Data processing system and method thereof; Micheal G. Gallup, et al., 395/588; 364/DIG.1 :IMAGE AVAILABLE:

21. 5,548,768, Aug. 20, 1996, Data processing system and method thereof;

Michael G. Gallup, et al., 395/376; 364/DIG.1 :IMAGE AVAILABLE:

22. 5,539,479, Jul. 23, 1996, Video receiver display of cursor and menu
overlaying video; Randal L. Bertram, 348/564; 345/120, 158; 348/601, 734
:IMAGE AVAILABLE:

23. 5,530,662, Jun. 25, 1996, Fixed point signal **processor** having
block floating processing circuitry; Hisami Ide, 364/736.01 :IMAGE
AVAILABLE:

24. 5,517,436, May 14, 1996, Digital signal **processor** for audio
applications; David C. Andreas, et al., 364/736.04, 736.02, 768 :IMAGE
AVAILABLE:

25. 5,512,896, Apr. 30, 1996, Huffman encoding method, circuit and
system employing most significant bit change for size detection;
Christopher J. Read, et al., 341/65 :IMAGE AVAILABLE:

26. 5,509,129, Apr. 16, 1996, Long instruction word controlling plural
independent **processor** operations; Karl M. Guttag, et al., 395/379;
364/736.04; 395/800.24 :IMAGE AVAILABLE:

27. 5,508,951, Apr. 16, 1996, **Arithmetic** apparatus with overflow
correction means; Toshihiro Ishikawa, 364/745.03 :IMAGE AVAILABLE:

28. 5,479,166, Dec. 26, 1995, Huffman decoding method, circuit and
system employing conditional subtraction for conversion of negative
numbers; Christopher J. Read, et al., 341/65 :IMAGE AVAILABLE:

29. 5,426,600, Jun. 20, 1995, **Double precision** division circuit
and method for digital signal **processor**; Tetsuya Nakagawa, et al.,
364/764, 761, 766 :IMAGE AVAILABLE:

30. 5,400,403, Mar. 21, 1995, Abuse-resistant object distribution system
and method; Paul N. Fahn, et al., 380/21, 4, 25 :IMAGE AVAILABLE:

31. 5,388,236, Feb. 7, 1995, Digital signal **processor** with multiway
branching based on parallel evaluation of N threshold values followed by
sequential evaluation of M; Tokumichi Murakami, et al., 395/583;
364/221.4, 261.5, DIG.1; 395/800.36 :IMAGE AVAILABLE:

32. 5,359,674, Oct. 25, 1994, Pyramid **processor** integrated circuit;
Gooitzen S. van der Wal, 382/261, 240, 299 :IMAGE AVAILABLE:

33. 5,307,506, Apr. 26, 1994, High bandwidth multiple computer bus
apparatus; Robert P. Colwell, et al., 395/307; 364/229, 240, 240.2,
240.5, DIG.1; 395/287 :IMAGE AVAILABLE:

34. 5,267,186, Nov. 30, 1993, Normalizing pipelined **floating
point** processing unit; Smeeta Gupta, et al., 364/748.14, 715.04,
748.13 :IMAGE AVAILABLE:

35. 5,233,698, Aug. 3, 1993, Method for operating data **processors**;
William S. Zuk, 395/560; 364/950, 950.3, DIG.2 :IMAGE AVAILABLE:

36. 5,222,230, Jun. 22, 1993, Circuitry for transferring data from a
data bus and temporary register into a plurality of input registers on
clock edges; Michael C. Gill, et al., 395/559; 364/228.6, 232.8, 238,
239, 239.7, 240, 247, 247.4, 247.6, 247.8, 258, 258.1, 258.2, 259, 259.2,
260, 260.2, 263, 265, 266.3, 271.9, DIG.1 :IMAGE AVAILABLE:

37. 5,187,799, Feb. 16, 1993, **Arithmetic**-stack **processor** which
precalculates external stack address before needed by **CPU** for
building high level language **executing** computers; Anthony McAuley, et
al., 395/800.36; 364/228.2, 231.8, 232.23, 232:3, 232.8, 238, 239, 239.8,

240, 244, 244.3, 245.7, 247, 247.3, 247.7, 247.8, 258, 258.1, 259, 259.1,
259.5, 262.4, 262.8, 2●●, 270, 270.4, 271.5, 280.4, DI● :IMAGE
AVAILABLE:

38. 5,062,041, Oct. 29, 1991, **Processor**/coprocessor interface
apparatus including microinstruction clock synchronization; William S.
Zuk, 395/562; 364/228, 228.6, 240.3, 262.4, 262.7, 262.8, 270, 270.3,
270.5, 271, 271.6; 395/553, 800.34 :IMAGE AVAILABLE:

39. 5,058,048, Oct. 15, 1991, Normalizing pipelined **floating
point** processing unit; Smeeta Gupta, et al., 364/748.14, 748.13
:IMAGE AVAILABLE:

40. 5,053,631, Oct. 1, 1991, Pipelined **floating point** processing
unit; Robert M. Perlman, et al., 364/748.14 :IMAGE AVAILABLE:

41. RE 33,629, Jul. 2, 1991, Numeric data **processor**; John F. Palmer,
et al., 364/748.16, 258, 715.08, 737, 748.02 :IMAGE AVAILABLE:

42. 5,029,069, Jul. 2, 1991, Data **processor**; Ken Sakamura, 395/581;
364/259, 261.5, 736.5 :IMAGE AVAILABLE:

43. 4,975,868, Dec. 4, 1990, **Floating-point processor** having
pre-adjusted exponent bias for multiplication and division; Donald L.
Freerksen, 364/748.09, 748.1 :IMAGE AVAILABLE:

44. 4,949,247, Aug. 14, 1990, System for transferring multiple vector
data elements to and from vector memory in a single operation; R. Ashley
Stephenson, et al., 395/800.06; 364/228, 228.1, 231.4, 231.8, 232.21,
236.8, 238, 238.4, 239, 239.4, 241.9, 242.6, 242.8, 244, 244.8, 247,
247.4, 256.3, 256.5, 258, 259, 259.9, 271, 271.2, 736.03, DIG.1;
395/800.07 :IMAGE AVAILABLE:

45. 4,947,359, Aug. 7, 1990, Apparatus and method for prediction of zero
arithmetic/logic results; Stamatis Vassiliadis, et al., 364/715.09,
736.5 :IMAGE AVAILABLE:

46. 4,945,479, Jul. 31, 1990, Tightly coupled scientific processing
system; John T. Rusterholz, et al., 395/800.03; 364/228, 228.1, 228.6,
228.9, 230, 230.3, 232.21, 239.9, 243, 243.1, 255.1, 280, 281.3, DIG.1
:IMAGE AVAILABLE:

47. 4,924,422, May 8, 1990, Method and apparatus for modified carry-save
determination of **arithmetic**/logic zero results; Stamatis Vassiliadis,
et al., 364/715.09, 736.5 :IMAGE AVAILABLE:

48. 4,916,651, Apr. 10, 1990, Floating point **processor** architecture;
Michael C. Gill, et al., 364/748.13, 750.5 :IMAGE AVAILABLE:

49. 4,901,268, Feb. 13, 1990, Multiple function data **processor**;
James E. Judd, 364/748.19, 749 :IMAGE AVAILABLE:

50. 4,875,161, Oct. 17, 1989, Scientific **processor** vector file
organization; Archie E. Lahti, 395/484; 364/222.81, 231.8, 232.21, 243.1,
246, 246.3, 252, 254, 254.2, 254.3, 263, 268.5, 271.6, 736.03, DIG.1;
395/405, 496 :IMAGE AVAILABLE:

51. 4,873,630, Oct. 10, 1989, Scientific **processor** to support a host
processor referencing common **memory**; John T. Rusterholz, et al.,
395/800.03; 364/228.1, 228.3, 231.8, 232.21, 232.7, 258, 258.1, 258.2,
263, DIG.1; 395/800.05, 800.06, 800.09 :IMAGE AVAILABLE:

52. 4,858,115, Aug. 15, 1989, Loop control mechanism for scientific
processor; John T. Rusterholz, et al., 395/800.07; 364/228.1, 228.2,
228.5, 228.6, 229, 229.1, 231.9, 232.21, 232.22, 232.7, 238.5, 239.4,

241.9, 242.6, 242.91, 243, 244.3, 246, 246.3, 247, 247.8, 259.9, 262, 262.1, 265, 265.3, 271, 271.2, 271.6, 927.92, 927.95, 92⬤931, 931.4, 931.51, 937.1, 937.7, 938, 938.1, 940, 940.4, 942.7, 943⬤, 946.8, 950, 950.3, 964, 965.4, 966.1, 966.4, 977, DIG.1, DIG.2; 395/800.04 :IMAGE AVAILABLE:

53.   4,852,048, Jul. 25, 1989, Single instruction multiple data (SIMD) cellular array processing apparatus employing a common bus where a first number of bits manifest a first bus portion and a second number of bits manifest a second bus portion; Steven G. Morton, 395/800.11; 364/228.6, 229, 229.4, 231.9, 232.8, 232.9, 238, 240, 240.1, 244, 244.6, 244.8, 244.9, 245, 245.3, 247, 247.8, 256.3, 265, 266.3, 267, 267.7, 268, 268.9, 280, 280.2, 280.3, DIG.1; 395/800.22 :IMAGE AVAILABLE:

54.   4,833,599, May 23, 1989, Hierarchical priority branch handling for parallel **execution** in a parallel **processor**; Robert P. Colwell, et al., 395/583; 364/228.3, 231.8, 242.3, 242.6, 242.7, 247, 258, 258.1, 258.2, 259, 261.3, 261.5, 261.9, 262.4, 262.9, DIG.1; 395/800.24 :IMAGE AVAILABLE:

55.   4,797,808, Jan. 10, 1989, Microcomputer with self-test of macrocode; Jeffrey D. Bellay, et al., 395/183.06; 364/228.6, 232.8, 232.9, 240,. 240.2, 244, 244.8, 245, 245.31, 245.4, 246.91, 247, 247.3, 247.6, 249, 249.2, 252, 258, 262.4, 262.7, 262.8, 265, 265.6, 266.3, 270, 270.3, 271.6, DIG.1 :IMAGE AVAILABLE:

56.   4,794,517, Dec. 27, 1988, Three phased pipelined signal **processor**; Gardner D. Jones, et al., 395/800.32; 364/221, 221.4, 231.8, 232.8, 232.9, 238, 239, 239.51, 240, 240.1, 240.2, 241.9, 242.3, 242.31, 242.32, 243, 243.3, 244, 244.3, 244.8, 247, 247.3, 247.8, 252, 254, 254.5, 258, 258.2, 259, 259.9, 260.4, 260.8, 261, 261.1, 262, 262.1, 262.4, 263, 263.2, 267, 267.5, 267.8, 270, 270.4, 271.6, 271.7, DIG.1 :IMAGE AVAILABLE:

57.   4,791,590, Dec. 13, 1988, High performance signal **processor**; Walter H. Ku, et al., 364/726.02, 726.06, 736.02 :IMAGE AVAILABLE:

58.   4,791,403, Dec. 13, 1988, Log encoder/decorder system; Joan L. Mitchell, et al., 341/51, 63, 75; 364/715.02, 748.01, 748.5, 857 :IMAGE AVAILABLE:

59.   4,777,613, Oct. 11, 1988, **Floating point** numeric data **processor**; Van B. Shahan, et al., 364/748.16, 223, 224, 228.6, 240, 240.2, 240.7, 244, 244.9, 258, 258.4, 262.4, 262.8, DIG.1 :IMAGE AVAILABLE:

60.   4,760,525, Jul. 26, 1988, Complex **arithmetic** vector **processor** for performing control function, scalar operation, and set-up of vector signal processing instruction; Richard F. Webb, 395/800.02; 364/DIG.1 :IMAGE AVAILABLE:

61.   4,748,580, May 31, 1988, **Multi-precision** fixed/floating-point **processor**; Charles D. Ashton, et al., 364/748.19 :IMAGE AVAILABLE:

62.   4,694,398, Sep. 15, 1987, Digital image frame **processor**; Francis R. Croteau, 382/309; 378/901 :IMAGE AVAILABLE:

63.   4,680,701, Jul. 14, 1987, Asynchronous high speed **processor** having high speed memories with domino circuits contained therein; Michael J. Cochran, 395/800.4; 364/232.8, 236.2, 237.2, 237.3, 238, 243, 243.6, 246.13, 246.3, 258, 270, 270.4, 270.5, 270.9, 271.5, 281.3, DIG.1; 365/194, 233 :IMAGE AVAILABLE:

64.   4,672,360, Jun. 9, 1987, Apparatus and method for converting a

number in binary format to a decimal format; John J. Bradley, et al.,
341/104; 364/715.011 : IMAGE AVAILABLE:

65. 4,667,190, May 19, 1987, Two axis fast access memory; Karl M.
Fant, 345/200 :IMAGE AVAILABLE:

66. 4,638,450, Jan. 20, 1987, Equal nine apparatus for supporting
absolute value subtracts on decimal operands of unequal length; Brian L.
Stoffers, 364/715.011, 768 :IMAGE AVAILABLE:

67. 4,627,021, Dec. 2, 1986, Integrated processor for the processing
of word-wise receivable data; Eric H. J. Persoon, et al., 395/800.36;
364/927.8, 933, 933.1, 937.1, 937.4, 937.8, 940, 942, 942.03, 947, 947.6,
957, 957.1, 957.8, 966.1, 966.7, DIG.2 :IMAGE AVAILABLE:

68. 4,620,287, Oct. 28, 1986, Method and apparatus for representation of
a curve of uniform width; David S. Yam, 395/142; 345/136; 396/556 :IMAGE
AVAILABLE:

69. 4,615,016, Sep. 30, 1986, Apparatus for performing simplified
decimal multiplication by stripping leading zeroes; John J. Bradley, et
al., 364/756, 754.01 :IMAGE AVAILABLE:

70. 4,608,659, Aug. 26, 1986, Arithmetic logic unit with outputs
indicating invalid computation results caused by invalid operands; John
J. Bradley, et al., 364/737 :IMAGE AVAILABLE:

71. 4,604,722, Aug. 5, 1986, Decimal arithmetic logic unit for
doubling or complementing decimal operand; Theodore R. Staplin, Jr., et
al., 364/715.011, 754.01 :IMAGE AVAILABLE:

72. 4,580,216, Apr. 1, 1986, Microcomputer with internal selection of
on-chip or off-chip access; Jeffrey D. Bellay, et al., 395/800.37;
364/232.8, 240, 240.2, 247, 247.8, 254.8, 258, 259, 262, 262.2, 262.4,
262.7, 262.8, DIG.1 :IMAGE AVAILABLE:

73. 4,580,215, Apr. 1, 1986, Associative array with five arithmetic
paths; Steven G. Morton, 395/800.13; 364/229, 229.5, 231.9, 238, 238.6,
238.7, 238.8, 240, 240.2, 244, 244.2, 244.8, 253, 253.3, 258, 258.4, 259,
259.5, 259.6, 716.03, 736.5, DIG.1 :IMAGE AVAILABLE:

74. 4,562,537, Dec. 31, 1985, High speed processor; Howard S.
Barnett, et al., 395/562; 364/232.7, 232.8, 234, 235, 236.2, 237.2,
237.3, 237.8, 238, 240, 240.2, 242.4, 243, 244, 244.3, 244.6, 246, 246.3,
248.1, 252, 258, 259, 259.8, 260, 260.2, 263.1, DIG.1; 395/800.32 :IMAGE
AVAILABLE:

75. 4,495,563, Jan. 22, 1985, Microcomputer having separate access to
complete microcode words and partial microcode words; Kevin C. McDonough,
395/800.42; 364/232.8, 243, 243.3, 244, 244.6, 252, 262.4, 262.7, 262.8,
DIG.1 :IMAGE AVAILABLE:

76. 4,490,783, Dec. 25, 1984, Microcomputer with self-test of microcode;
Kevin C. McDonough, et al., 395/568; 364/232.8, 243, 244, 244.6, 252,
262.4, 262.7, 262.8, 267, DIG.1; 371/40.18; 395/595 :IMAGE AVAILABLE:

77. 4,484,259, Nov. 20, 1984, Fraction bus for use in a numeric data
processor; John Palmer, et al., 364/754.01, 736.01, 748.09, 761
:IMAGE AVAILABLE:

78. 4,471,426, Sep. 11, 1984, Microcomputer which fetches two sets of
microcode bits at one time; Kevin C. McDonough, 395/387; 364/232.7,
232.8, 236.2, 236.3, 244, 244.6, 247, 247.2, 247.3, 247.6, 251, 251.3,
253, 253.2, 258, 259, 259.9, 262.4, 262.7, 262.8, 263.1, 280, 280.9,
DIG.1; 395/598 :IMAGE AVAILABLE:

79. 4,467,444, Aug. 2? █984, **Processor** unit for micro█ █uter systems; William J. Har...n, Jr., et al., 395/800.42; 364█36.01, 926.1, 926.5, 931, 931.1, 933, 933.1, 933.62, 933.9, 934, 934.1, 937.1, 940, 942, 942.8, 947, 947.1, 947.4, 947.6, 948, 957, 957.4, 959, 965, 965.3, DIG.2; 395/561 :IMAGE AVAILABLE:

80. 4,455,602, Jun. 19, 1984, Digital data processing system having an I/O means using unique address providing and access priority control techniques; Ward Baxter, III, et al., 395/825; 364/228.1, 228.3, 231.4, 231.6, 232.1, 243, 243.3, 244, 244.3, 246.6, 262.4, 262.8, 263, 280, 280.4, 281.3, 281.4, DIG.1; 395/859, 885 :IMAGE AVAILABLE:

81. 4,450,525, May 22, 1984, Control unit for a functional **processor**; Gordon L. Demuth, et al., 395/590; 364/221, 221.4, 221.5, 224, 224.2, 230, 230.3, 231.8, 238.4, 239, 239.1, 244, 244.3, 244.4, 244.6, 244.8, 247, 247.2, 254, 254.3, 254.5, 258, 258.1, 258.2, 259, 259.5, 260, 260.2, 261.3, 261.9, 262, 262.4, 262.8, 270.3, 280, 280.2, 281.3, DIG.1; 395/595, 733 :IMAGE AVAILABLE:

82. 4,450,521, May 22, 1984, Digital **processor** or microcomputer using peripheral control circuitry to provide multiple memory configurations and offset addressing capability; Kevin C. McDonough, et al., 395/823; 364/232.8, 232.9, 238.3, 239, 239.6, 240, 240.1, 240.2, 241.2, 241.6, 244, 244.1, 244.3, 244.5, 244.6, 245, 245.31, 245.4, 245.5, 246.91, 247, 247.2, 251, 251.3, 252, 258, 259, 259.9, 262.4, 262.8, 263.2, 270, DIG.1 :IMAGE AVAILABLE:

83. 4,449,196, May 15, 1984, Data processing system for **multi-precision arithmetic**; Eric K. Pritchard, 364/768, 745.01, 921, 921.2, 921.3, 921.8, 921.9, 926.9, 931.4, 931.44, 931.48, 935, 935.2, 935.4, 935.44, 937.1, 937.2, 937.7, 937.8, 939, 939.1, 939.4, 939.7, 940, 940.2, 941, 941.1, 942.3, 942.4, 942.5, 942.7, 942.8, 943.9, 944.6, 944.9, 946.2, 946.7, 948.2,ˋ 949, 950, 950.2, 950.3, 950.4, 950.61, 951.1, 951.4, 964, 964.5, 964.7, 966, 966.4, 967, 967.3, DIG.2 :IMAGE AVAILABLE:

84. 4,445,177, Apr. 24, 1984, Digital data processing system utilizing a unique arithmetic logic unit for handling uniquely identifiable addresses for operands and instructions; Richard G. Bratt, et al., 395/595; 364/228.3, 231.4, 231.6, 232.1, 238.4, 239, 239.7, 241.2, 241.3, 241.5, 241.9, 243, 243.4, 243.41, 243.43, 244, 244.3, 244.6, 246.6, 246.7, 246.8, 246.9, 246.91, 247, 247.2, 247.7, 247.8, 254, 254.3, 254.5, 256.8, 258, 258.2, 258.3, 259, 259.5, 259.8, 261.3, 261.6, 262.4, 262.7, 262.8, 262.81, 263, 263.2, 263.3, 265, 265.3, 266, 266.1, 267, 267.6, 267.9, 270, 270.1, 271, 271.3, 271.4, 271.6, 271.8, 280, 280.1, 280.4, 280.8, 280.9, 281, 281.3, 281.4, 281.5, 281.6, 281.7, 281.8, 282, 282.1, 282.2, 284, 284.3, DIG.1 :IMAGE AVAILABLE:

85. 4,441,154, Apr. 3, 1984, Self-emulator microcomputer; Kevin C. McDonough, et al., 395/800.43; 364/221, 221.6, 232.3, 232.8, 232.9, 238.6, 238.7, 239, 239.6, 240.1, 241.2, 241.6, 242, 244, 244.3, 244.6, 254, 254.3, 258, 260.4, 260.8, 261.3, 261.9, 262.4, 262.7, 262.8, 270, 270.4, DIG.1; 395/500, 733 :IMAGE AVAILABLE:

86. 4,423,483, Dec. 27, 1983, Data **processor** using a read only memory for selecting a part of a register into which data is written; Steven A. Tague, et al., 395/898; 364/228.6, 229, 229.2, 230, 230.3, 230.4, 240, 240.1, 240.2, 240.8, 240.9, 243, 243.4, 243.41, 252.3, 252.6, 255.1, 255.7, 258, 258.1, 258.2, 258.3, 259, 259.5, 259.6, 259.7, 264, 264.1, 264.5, DIG.1 :IMAGE AVAILABLE:

87. 4,390,961, Jun. 28, 1983, Data **processor** performing a decimal multiply operation using a read only memory; Virendra S. Negi, et al., 364/756 :IMAGE AVAILABLE:

88. 4,389,706, Jun. 2? ●983, Digital computer monitore● ●nd/or operated
system or process which ●s structured for operation with ●n improved
automatic programming process and system; John W. Gomola, et al.,
364/130, 226.7, 227.4, 231.4, 231.6, 237.8, 241.2, 241.3, 241.5, 259,
259.3, 260, 260.1, 260.4, 260.6, 281.3, 281.6, 281.8, 282.1, 282.3,
283.1, 468.03, 468.15, 492, 550, DIG.1 :IMAGE AVAILABLE:

89. 4,378,589, Mar. 29, 1983, Undirectional looped bus microcomputer
architecture; Edward D. Finnegan, et al., 395/310; 364/229, 229.2, ·231.8,
232.8, 238, 238.4, 239, 239.8, 240, 240.1, 240.2, 241.1, 241.2, 241.6,
241.9, 243, 244, 244.6, 247, 247.8, 258, 258.4, 259, 259.9, 260, 260.1,
262.4, 262.8, 263, 270, 270.4, 271.6, 271.7, 271.8, DIG.1 :IMAGE
AVAILABLE:

90. 4,339,793, Jul. 13, 1982, Function integrated, shared ALU
processor apparatus and method; George B. Marenin, 395/800.32;
364/229, 229.3, 231.4, 231.7, 231.8, 232.3, 232.8, 238, 240, 240.1,
240.2, 241.1, 241.2, 241.3, 241.5, 241.9, 242.3, 243, 243.3, 244, 244.3,
247, 247.1, 247.2, 247.3, 247.4, 251, 251.1, 252.3, 252.6, 255.1, 259,
259.7, 260, 260.1, 260.2, 261, 261.2, 261.3, 261.4, 261.5, 262.4, 262.8,
263, 263.1, 270, 270.3, 271.6, 271.7, DIG.1; 395/726 :IMAGE AVAILABLE:

91. 4,338,675, Jul. 6, 1982, Numeric data **processor**; John F. Palmer,
et al., 364/748.16, 224, 230, 230.4, 232.8, 240, 244, 244.3, 247, 247.8,
258, 258.1, 258.2, 258.3, 258.4, 259, 259.5, 259.7, 260.4, 260.9, 263,
263.1, 264, 264.2, 265, 265.4, 266.4, 271, 271.2, 715.08, 737, 748.02,
DIG.1 :IMAGE AVAILABLE:

92. 4,312,034, Jan. 19, 1982, ALU and Condition code control unit for
data **processor**; Thomas G. Gunter, et al., 395/595; 364/231.9, 238.6,
239, 239.3, 239.4, 241.2, 241.6, 242.1, 243, 243.3, 244, 244.6, 247,
247.6, 254, 254.2, 258, 258.1, 258.2, 258.3, 259, 259.1, 259.6, 259.9,
261.3, 261.5, 262.4, 262.6, 262.7, 262.8, 262.81, 262.9, 271.6, 271.8,
DIG.1 :IMAGE AVAILABLE:

93. 4,272,828, Jun. 9, 1981, **Arithmetic** logic apparatus for a data
processing system; Virendra S. Negi, et al., 364/736.01, 768, 927.8, 931,
931.1, 933, 933.1, 933.2, 933.3, 933.5, 933.61, 933.7, 935, 935.2, 935.4,
937, 937.1, 937.2, 938, 938.1, 939, 939.7, 940, 941, 941.1, 942, 942.04,
942.7, 942.8, 943.9, 945.3, 945.6, 946.2, 946.6, 946.9, 947, 947.1,
947.5, 947.6, 948, 948.1, 948.3, 950, 950.1, 950.3, 951.5, 954, 954.1,
957, 957.4, 958, 958.2, 958.3, 960, 960.6, 961.1, 962, 962.1, 965, 965.5,
965.8, DIG.2 :IMAGE AVAILABLE:

94. 4,262,336, Apr. 14, 1981, Multi-axis contouring control system; Eric
K. Pritchard, 364/474.11; 318/573, 696; 364/132, 174, 474.3, 474.31
:IMAGE AVAILABLE:

95. 4,247,893, Jan. 27, 1981, **Memory** interface device with
processing capability; Jack L. Anderson, et al., 395/309; 364/238, 238.3,
238.4, 239, 239.1, 239.3, 240, 240.5, 244, 244.6, 247, 247.2, 247.4,
247.5, 247.6, 247.7, 247.8, 255.1, 255.2, 255.5, 258, 258.1, 259, 259.1,
259.3, 259.5, DIG.1 :IMAGE AVAILABLE:

96. 4,227,245, Oct. 7, 1980, Digital computer monitored system or
process which is configured with the aid of an improved automatic
programming system; Warren A. Edblad, et al., 364/468.01, 221, 221.2,
221.7, 221.9, 222.81, 222.82, 224, 224.2, 230, 230.1, 230.3, 230.4, 234,
235, 237.2, 237.8, 238, 242.1, 245, 245.1, 248, 248.1, 248.3, 259, 259.5,
262.4, 262.5, 267.9, 280, 281.3, 281.7, 281.8, 282.1, 282.3, 283.1, DIG.1
:IMAGE AVAILABLE:

97. 4,215,407, Jul. 29, 1980, Combined file and directory system for a
process control digital computer system; John W. Gomola, et al.,

364/468.01, 221, 221.2, 221.4, 221.7, 221.9, 222.81, 226.8, 226.9, 228.3, 230, 230.1, 230.2, 230 230.4, 232.3, 234, 235, 236.1, .2, 236.3, 237.2, 237.4, 237.8, 24..1, 248, 248.1, 248.3, 254.9, 25 1, 255.2, 258, 258.1, 258.2, 258.3, 259, 259.5, 262.4, 262.5, 264, 280, 280.8, 281.3, 281.7, 281.8, DIG.1 :IMAGE AVAILABLE:

98.   4,215,406, Jul. 29, 1980, Digital computer monitored and/or operated system or process which is structured for operation with an improved automatic programming process and system; John W. Gomola, et al., 364/468.01, 221, 221.2, 221.4, 221.7, 221.9, 222, 222.81, 222.82, 230, 230.1, 230.3, 234, 237.8, 238.2, 238.3, 241.2, 242.1, 243, 243.2, 245, 245.5, 246, 246.3, 248.1, 251, 251.5, 252, 259, 259.3, 260.4, 260.6, 260.9, 261, 262.4, 262.5, 267, 267.1, 267.2, 267.4, 270.5, 270.8, DIG.1 :IMAGE AVAILABLE:

99.   4,202,035, May 6, 1980, Modulo addressing apparatus for use in a microprocessor; John H. Lane, 395/421.07; 364/223, 223.7, 224, 224.1, 224.2, 238.6, 238.7, 238.8, 240, 240.1, 240.2, 244, 244.3, 251, 251.5, 262, 262.1, 262.4, 262.5, 262.7, 270, 270.1, 736.5, DIG.1 :IMAGE AVAILABLE:

100.   4,201,908, May 6, 1980, Measurement and recording apparatus and system; Bernard A. Johnson, et al., 377/9; 340/941; 377/6, 26 :IMAGE AVAILABLE:

101.   4,181,934, Jan. 1, 1980, Microprocessor architecture with integrated interrupts and cycle steals prioritized channel; George B. Marenin, 395/860; 364/231.4, 231.8, 232.3, 232.8, 238, 240, 240.1, 241.1, 241.2, 241.5, 241.9, 242.3, 242.31, 243, 243.3, 244, 244.3, 244.6, 245, 245.1, 247, 247.1, 247.2, 247.3, 247.6, 247.8, 251, 251.1, 252.3, 252.6, 254, 254.4, 254.6, 255, 255.1, 255.7, 258, 259, 259.1, 259.4, 259.5, 259.7, 260, 260.1, 261, 261.2, 261.3, 261.4, 261.5, 262.4, 262.5, 262.8, 263, 263.1, 263.2, 264, 264.4, 264.6, 265, 265.5, 266.3, 270, 270.3, 270.5, 270.6, 271.6, 271.7, DIG.1; 395/858 :IMAGE AVAILABLE:

102.   3,872,442, Mar. 18, 1975, SYSTEM FOR CONVERSION BETWEEN CODED BYTE AND **FLOATING POINT** FORMAT; John A. Boles, et al., 364/715.03, 231.9, 232.7, 243, 243.2, 243.6, 248.3, 260.4, 260.9, DIG.1 :IMAGE AVAILABLE:

103.   3,766,370, Oct. 16, 1973, ELEMENTARY **FLOATING POINT** CORDIC FUNCTION **PROCESSOR** AND SHIFTER; John S. Walther, 364/747, 231, 231.3, 232.9, 232.93, 244, 244.6, 258, 258.1, 258.2, 258.3, 258.4, 262.4, 262.8, 7.16.01, 719, 721, 722, DIG.1 :IMAGE AVAILABLE:

104.   3,739,352, Jun. 12, 1973, VARIABLE WORD WIDTH **PROCESSOR** CONTROL; Roger E. Packard, 395/421.04; 364/238.4, 240.1, 243, 243.3, 243.7, 245, 245.1, 251, 251.1, 251.3, 252.3, 252.6, 254.9, 255.1, 255.5, 258, 258.1, 259, 259.3, 259.5, 260, 260.2, 261.3, 261.9, 262.4, 262.8, DIG.1 :IMAGE AVAILABLE:

105.   3,702,393, Nov. 7, 1972, CASCADE DIGITAL FAST FOURIER ANALYZER; Peter Siegfried Fuss, 364/726.02; 324/76.21, 76.35; 364/726.04 :IMAGE AVAILABLE:

106.   3,701,976, Oct. 31, 1972, **FLOATING POINT ARITHMETIC** UNIT FOR A PARALLEL PROCESSING COMPUTER; Richard Robert Shively, 364/715.08, 223, 223.1, 225, 227, 227.2, 229, 229.2, 230, 230.3, 230.4, 231.9, 258, 258.2, 258.4, 259, 259.4, 259.5, 259.7, 260.4, 260.9, 271.6, 271.7, 768, DIG.1 :IMAGE AVAILABLE:

107.   3,626,427, Dec. 7, 1971, LARGE-SCALE DATA PROCESSING SYSTEM; Olin L. MacSorley, et al., 395/591; 364/231.4, 234, 237.2, 237.4, 241.2, 241.3, 246.6, 246.8, 258, 262, 263.1, 265, 266, 266.3, 270, DIG.1; 395/569 :IMAGE AVAILABLE: